CLAIMS

What is claimed is:

1. A method of manufacturing a semiconductor component, the method comprising:

providing a semiconductor substrate having a surface and a first conductivity type;

forming a trench in the surface of the semiconductor substrate to define a plurality of active areas separated from each other by the trench;

forming a buried layer in the semiconductor substrate underneath a portion of the trench, wherein the buried layer has a second conductivity type and is at least partially contiguous with the trench;

after forming the buried layer, depositing an electrically insulating material in the trench;

forming a collector region having the second conductivity type in one of the plurality of active areas;

forming a base structure having the first conductivity type over the one of the plurality of active areas; and

forming an emitter region having the second conductivity type over the one of the plurality of active areas,

wherein:

the collector region forms a contact to the buried layer.

2. The method of claim 1 wherein:

the collector region has a first resistivity;

the buried layer has a second resistivity; and

the first resistivity is greater than the second resistivity.

3. The method of claim 1 further comprising:

forming a spacer structure in the trench; and

after forming the buried layer, removing the spacer structure.

4. The method of claim 1 wherein:

forming the buried layer comprises:

implanting a dopant having the second conductivity type through the trench.

5. The method of claim 4 wherein:

forming the buried layer further comprises:

annealing the dopant after implanting the dopant and before filling the trench.

6. The method of claim 1 wherein:

forming the buried layer comprises:

self-aligning the buried layer to the trench.

7. The method of claim 1 wherein:

the semiconductor substrate comprises a semiconductor region of a first kind and a semiconductor region of a second kind;

the method further comprises forming an implant mask over the semiconductor region of the second kind before forming the buried layer; and

forming the buried layer further comprises:

forming the buried layer underneath at least a portion of the trench in semiconductor region of the first kind.

8. The method of claim 7 wherein:

the semiconductor region of the first kind comprises a bipolar semiconductor region; and

the semiconductor region of the second kind comprises a CMOS region.

9. The method of claim 1 wherein:

manufacturing the semiconductor component comprises:

manufacturing the one of the plurality of active areas to be symmetric about a vertical line drawn through a middle of the emitter region.

10. A semiconductor component formed by the method of claim 1.

11. A method of manufacturing a semiconductor component, the method comprising:

providing a semiconductor substrate having a surface and a first conductivity type, where the semiconductor substrate comprises a plurality of semiconductor regions of a first kind and a plurality of semiconductor regions of a second kind;

forming a trench in the surface of the semiconductor substrate to define a plurality of active areas separated from each other by the trench;

performing a buried layer module comprising:

forming a plurality of spacer structures in the trench;

forming an implant mask over the plurality of semiconductor regions of the second kind; and

forming a plurality of buried layers, each one of the plurality of buried layers located underneath at least a portion of the trench in the plurality of semiconductor regions of the first kind, where the plurality of buried layers have a second conductivity type, are at least partially contiguous with the trench, and one of the plurality of spacer structures is used to self-align one of the plurality of buried layers to the trench;

after forming the plurality of buried layers, depositing an electrically insulating material in the trench;

forming a collector region having the second conductivity type in each of the plurality of semiconductor regions of the first kind; and

forming an emitter region having the second conductivity type over each of the plurality of semiconductor regions of the first kind,

wherein:

the collector region in each one of the plurality of semiconductor regions of the first kind forms a contact to the buried layer in the one of the plurality of semiconductor regions of the first kind.

12. The method of claim 11 further comprising:

removing the plurality of spacer structures after forming the plurality of buried layers.

13. The method of claim 11 further comprising:

forming a base region having the second conductivity type in the plurality of semiconductor regions of the first kind.

14. The method of claim 13 wherein:

forming the base region further comprises:

forming a contact in the base region; and

the contact in the base region is above at least a portion of the trench.

15. The method of claim 11 wherein:

the collector region has a first resistivity;

the plurality of buried layers have a second resistivity; and

the first resistivity is greater than the second resistivity.

16. The method of claim 11 wherein:

forming the plurality of buried layers comprises:

implanting a dopant having the second conductivity type through the trench.

17. The method of claim 16 wherein:

forming the plurality of buried layers further comprises:

annealing the dopant after implanting the dopant and before filling the trench.

18. The method of claim 11 wherein:

manufacturing the semiconductor component comprises:

manufacturing the plurality of semiconductor regions of the first kind to be symmetric about a vertical line drawn through a middle of the emitter region.

19. The method of claim 11 wherein:

the buried layer module is compatible with a CMOS process flow.

20. A method of manufacturing a semiconductor component, the method comprising:

providing a semiconductor substrate having a surface and a first conductivity type, where the semiconductor substrate comprises a plurality of bipolar semiconductor regions and a plurality of CMOS regions;

forming a trench in the surface of the semiconductor substrate in the plurality of bipolar semiconductor regions and in the plurality of CMOS regions to define a plurality of active areas separated from each other by the trench;

forming a buried layer in the semiconductor substrate underneath a portion of the trench in the plurality of bipolar semiconductor regions, where the buried layer has a second conductivity type and is at least partially contiguous with the trench;

after forming the buried layer, depositing an electrically insulating material in the trench;

forming a collector region having the second conductivity type in each one of the plurality of bipolar semiconductor regions;

forming a base structure having the first conductivity type over each one of the plurality of bipolar semiconductor regions;

forming an emitter having the second conductivity type over each one of the plurality of bipolar semiconductor regions;

forming source/drain regions over each one of the plurality of CMOS regions; and

forming a gate region over each one of the plurality of CMOS regions,

wherein:

the collector region forms a contact to the buried layer.

21. The method of claim 20 wherein:

forming the collector region occurs simultaneously with forming the source/drain regions.

22. The method of claim 20 wherein:

the collector region has a first resistivity;

the buried layer has a second resistivity; and

the first resistivity is greater than the second resistivity.

23. A semiconductor component formed by the method of claim 20.